Beyond Chip Stacking: Quilt Packaging Enabled 3D Systems

Speaker: **Jason Kulick** – Indiana Integrated Circuits, LLC, South Bend, IN

E-Mail: jason.kulick@indianaic.com

Abstract

Quilt Packaging is an edge interconnect technology for direct chip-to-chip integration. Quilt Packaging (QP) utilizes solid metal structures that protrude from the vertical sidewalls of chips and/or interposers, acting as both an electrical and mechanical interconnect. Electrically, Quilt Packaging performs as if it were an on-chip interconnect, demonstrating less than 1 dB insertion loss across the entire bandwidth from DC to 220 GHz. Mechanically, Quilt Packaging enables sub-micron chip-to-chip alignment accuracy and can also be completely customized for I/O ranging from 10 micron pitch to structures that measure in the hundreds of microns. QP technology can be implemented in variety of material and process technologies to enable true heterogeneous integration in planar and unique 3D configurations beyond chip stacking. Applications such as VCSEL integration, curved focal plane arrays and unique system miniaturization concepts enabled by Quilt Packaging will be discussed.